IDEC Chip Design Contest

Design of a broadband phase shifter and a dedicated LDO for 6G applications

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• Introduction

- ✓ Multi-state delay cell and LDO fabricated using a 28nm FD-SOI fabrication.
- ✓ A multi-state delay cell with three different states is designed for operation over the 4–12 GHz frequency range.
- ✓ Design of a BGR with a stable reference voltage and a high-PSRR LDO.

• Description

◆ Multi-state delay cell design

- ✓ Recently, true time delay (TTD) has gained increasing importance for broadband beamforming applications, although its bulky size remains a significant challenge for practical implementation.
- ✓ To address this issue, a multi-state delay cell capable of realizing multiple delay states within a single delay cell through switching functionality was designed, as shown in Fig. 1.

◆ Simulation and measurement result

- ✓ The group delay characteristics can be controlled depending on the on/off state of the transistor, and the measurement results show good agreement with the simulation results over the 4–12 GHz frequency range.
- ✓ However, the large parasitic Ron of the transistor and the narrow metal width result in significant insertion loss, requiring further improvement.

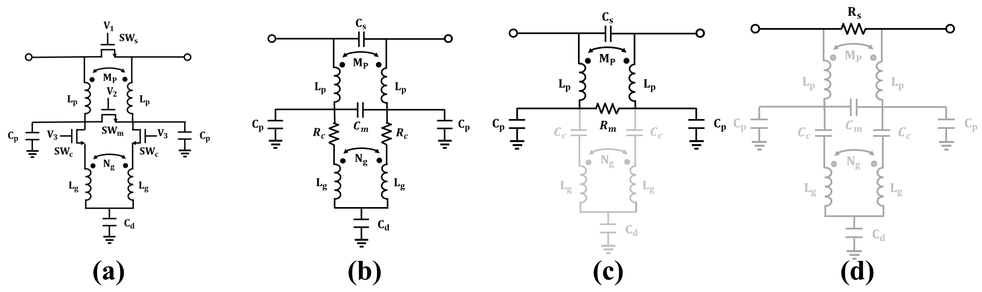

Fig 1. (a) schematic of multi-state delay and equivalent circuit of (b) large, (c) medium, (d) small delay state

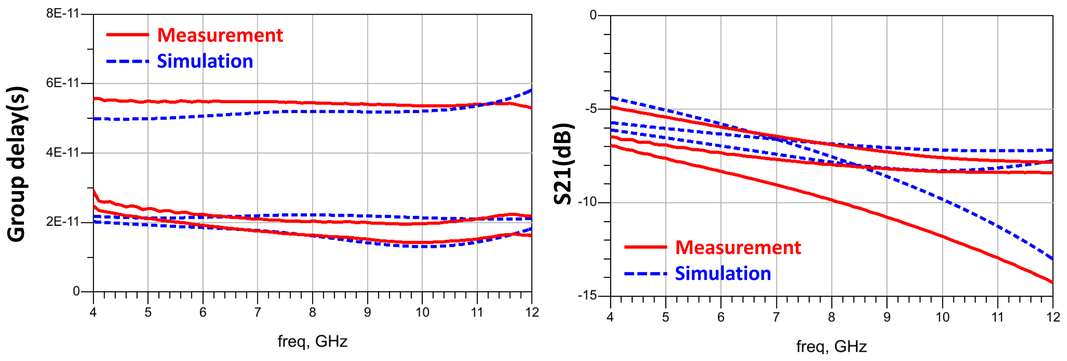

Fig 2. Simulation and Measurement result of TTD

◆ LDO and BGR design

- ✓ To ensure a stable output, the LDO compares the feedback voltage with a BGR via an error amplifier and compensates for any voltage differences.
- ✓ By integrating CTAT and PTAT behaviors, the BGR can output a stable, temperature-insensitive voltage, serving as a reliable voltage reference circuit over a specific temperature range.
- ✓ Input voltage: 1.8 V / Output voltage: 1.2 V

◆ Simulation and Measurement result

- ✓ Measurement results show an output voltage variation of approximately 0.06 V, but it is confirmed that the LDO generally maintains a stable 1.2 V output.
- ✓ Furthermore, the measured line regulation was 18.2 mV/V, which is significantly degraded compared to the simulated value of 0.82 mV/V; this discrepancy is suspected to be due to noise from the measurement equipment.

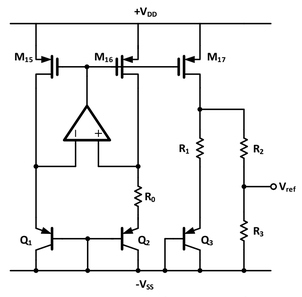

Fig 3. schematic of BGR & LDO

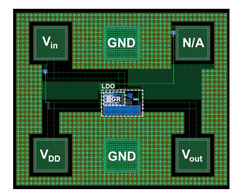

Fig 4. Layout of LDO

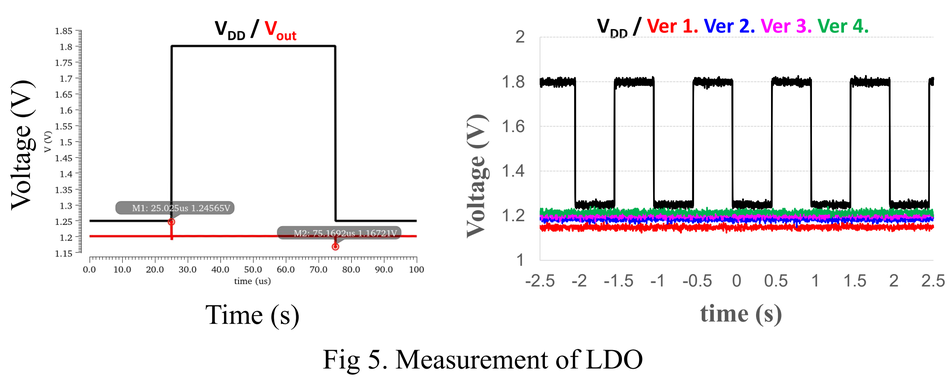

Fig 5. Measurement of LDO

• Conclusion

- ✓ The proposed multi-state delay cell successfully demonstrates three different delay states over 4–12 GHz, showing good agreement between simulation and measurement result.
- ✓ The LDO operates with an input voltage of 1.8 V and an output voltage of 1.2 V, featuring a line regulation of 20 mV/V or less.
- ✓ Based on the LDO for stable voltage supply and the multi-state delay cell for a compact size, a more stable and miniaturized 6G system can be implemented.